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CVD1

2D COMB FILTER NTSC/PAL/SECAM VIDEO DECODER

Product Brief

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Overview

Zoran's CVD1 Video Decoder is a silicon efficient, cost effective, high video quality Intellectual Property Core for IC designs requiring video input. The CVD2 decodes NTSC/PAL/SECAM composite video or S-video and converts it into YUV 4:2:2, 16-bit digital video.

Employing adaptive 2D comb filter technology, the CVD1 is able to provide high quality Y/C separation while maintaining excellent frequency response. The result is sharp, high detail video that eliminates unwanted dot crawl and false color effects. A fully digital design, the CVD1 requires the addition of only an A/D (two for S-Video support), a DC restore circuit and line buffers for implementation.

CVD1 is based on Zoran's extensive experience delivering high quality, high volume video ICs to major OEMs worldwide. Proven in silicon, the CVD1 Video Decoder greatly reduces the risk and time involved when integrating the video decoding function into an IC.

Deliverables

- RTL (Verilog) source code
- Bit accurate C++ model
- Synopsis synthesis scripts
- Test input files
- Documentation
- FPGA evaluation board available

Features

- Decodes NTSC, PAL or SECAM composite video or S-Video into the YUV 4:2:2 format
- Component video inputs supported
- Decodes all variations of the NTSC standard
- Decodes all variations of PAL standard
  – (I, B, G, H, D, N, M, combination N)
- Excellent quality Y/C separation
  – minimizes cross luma and cross color effects
- Superior frequency response preserves fine detail
- Accepts up to 11-bit inputs from A/D converter
- Digital automatic gain control (AGC) supported
- Adaptive 2D Comb Filter provides high quality video:
  – 3-line 2D Comb Filter for NTSC & PAL
  – 5-line 2D Comb Filter for PAL (optional)
- Auto-detects video standard (NTSC, PAL or SECAM)
- Auto-detects and locks to VCR trick modes
- Decodes weak and noisy off-air signals
- VBI decoding supported
- Silicon efficient design of approximately 130k gates
- Requires only a single clock input ranging from 20 to 30 MHz
- Process technology independent, fully synchronous design

Figure 1. Block Diagram of the CVD1 Intellectual Property Core

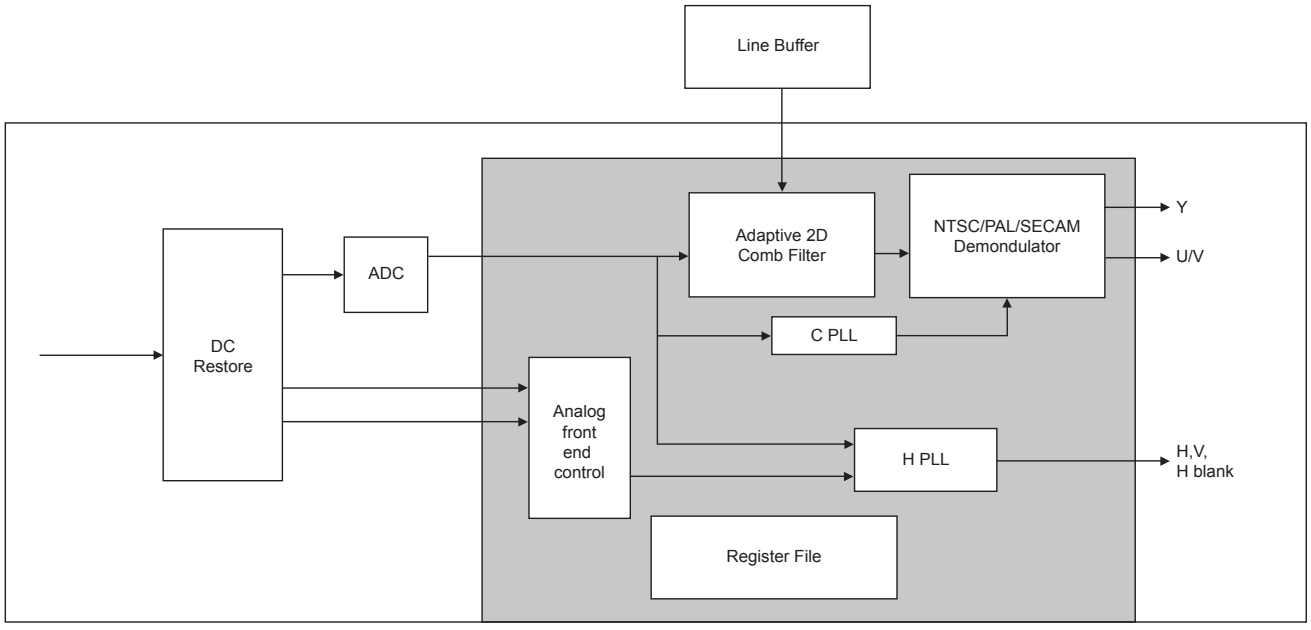

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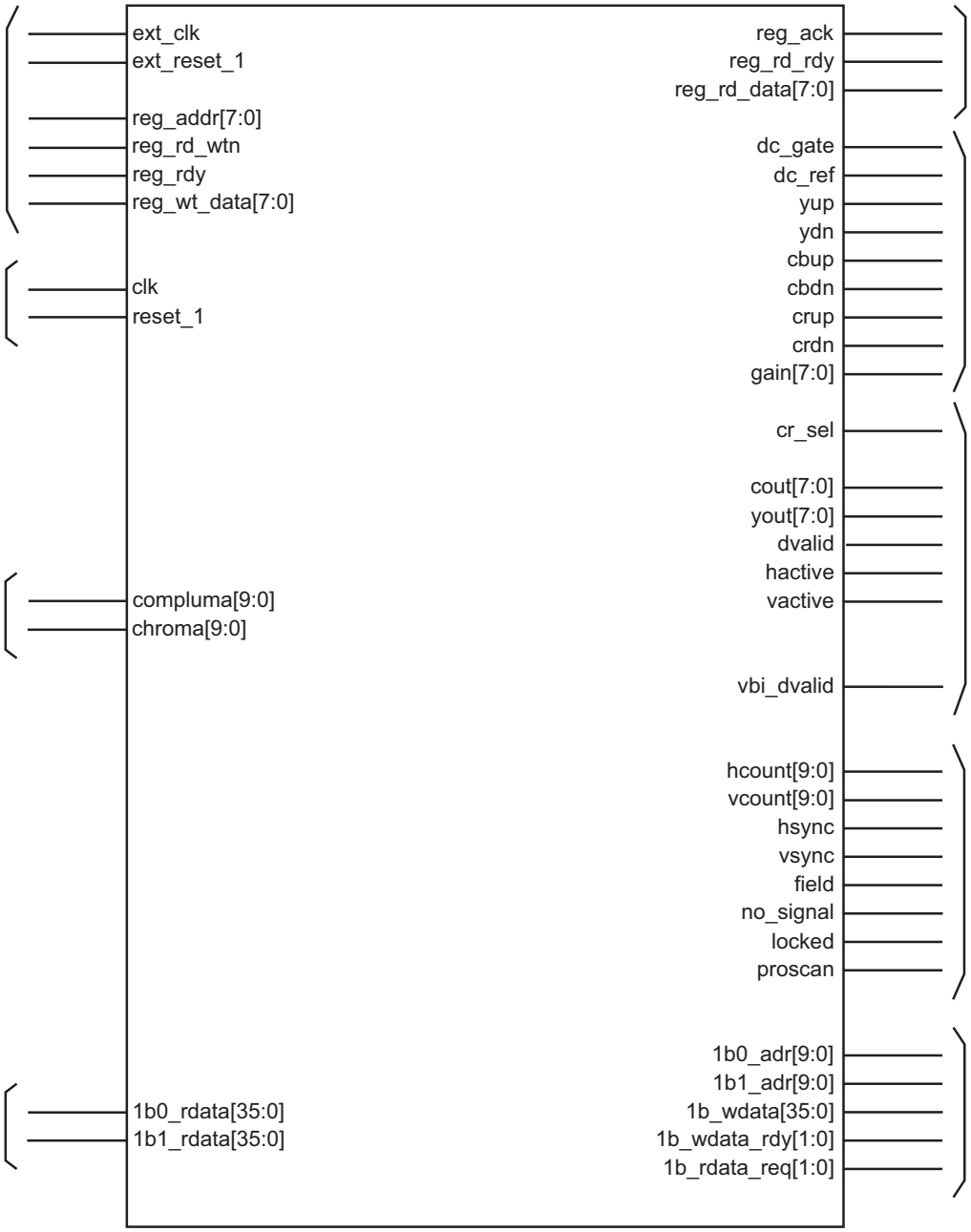
Figure 2. CVD1 Logical Pinout



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