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CVE2

DIGITAL PRINTING

NTSC/PAL VIDEO ENCODER

MOBILE

IP CORES

Product Brief

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Overview

Zoran's CVE2 NTSC/PAL video encoder core continues a line of highly efficient, cost effective solutions for the digital video market.

The CVE2 core encodes YCrCb video into all NTSC and PAL standards with full programmable timing parameters. The carrier frequency and phase provides maximum flexibility.

This synthesizable intellectual property core accepts YCrCb video as specified by the CCIR-601 standard or full range YCrCb. All timing signals are generated within the core, synchronized to an external 27 MHz clock. In master mode the core provides Hblank and Vblank to the video source. In slave mode Hblank and Vblank are inputs. In slave mode the core can also be configured to accept multiplexed YCrCb as specified by the CCIR-656 standard.

Features

- Encodes YCrCb into NTSC or PAL/SECAM
- Supports all variations of NTSC encoding
- Supports all variations of PAL encoding (I, B, G, D, N, M and combination N)
- RGB SCART output with (MV)
- Component YUV output with (MV)
- Controlled (smooth) edges on Sync and Burst
- Adheres to CCIR 601, 604 and 656 specs; also adheres to SMTPE 253 spec
- Programmable Notch Filter

Applications

- PC Video
- Digital camera process

The outputs are 6 separate busses for Y, Composite, Chroma, and RGB. This allows for flexibility in connection and multiplexing to DACs.

Design Considerations

- Low silicon area: approximately 29,000 gates
- Fully synchronous design
- Technology independent. synthesizable to most CMOS libraries

Deliverables

- Compilable RTL source code
- Bit accurate C model
- Synopsis synthesis scripts
- Test input files
- IP core documentation
- FPGA evaluation board available
- Upsampled design minimizes sinx/x distortion and complexity of external analog filter
- Nominal sample rate is 27 Msample/s
- Advanced Trick Play Features including Zoom, Smooth Scan
- Flexible input configuration: can be timing slave or master
- Outputs 10 bit data to DACs
- Generic register programming port
- Controlled entry and exit of active video line
- Fully programmable RGB setup and sync
- WSS & CGMS Data Line Encoding

- PC Graphic
- Any system requiring TV output

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Figure 1. CVE2 Intellectual Property Core

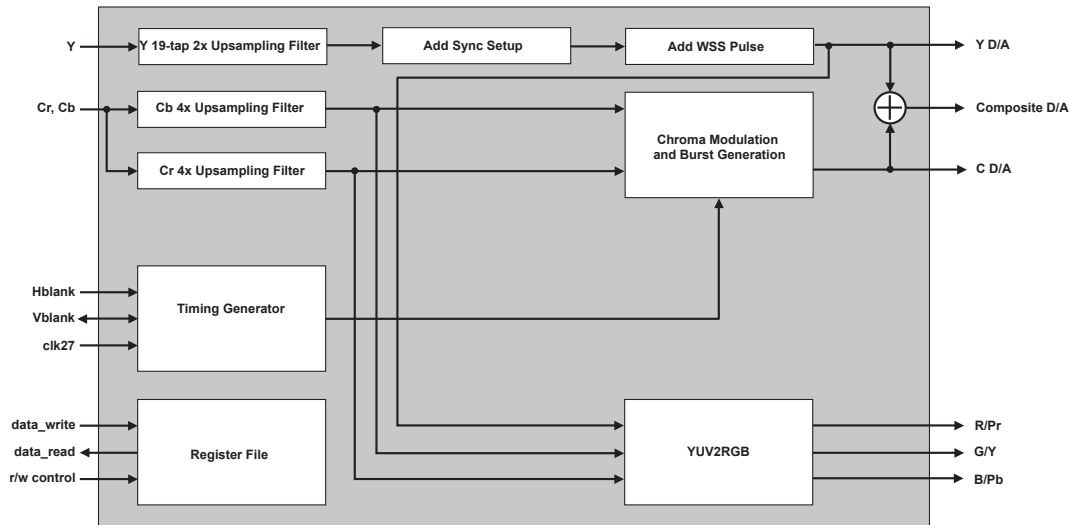


Figure 2. CVE2 Logical Pinout

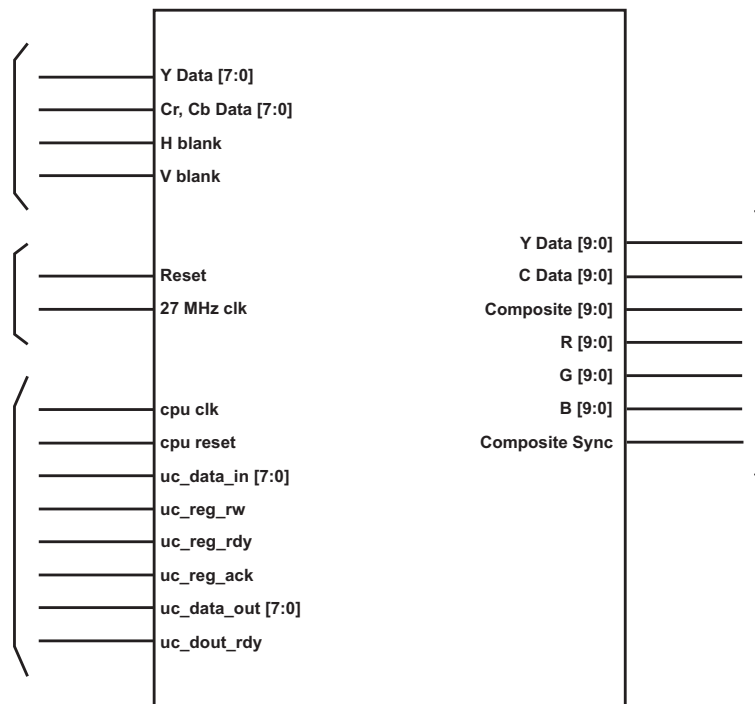


Figure 1. CVE2 Video Encoder Logical Pinout

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