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CVE5

HIGH DEFINITION VIDEO ENCODER

Product Brief

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Overview

Zoran's CVE5 High Definition Video Encoder is a silicon-efficient, high-quality Intellectual Property Core for video IC designs requiring the high definition TV encoding. The CVE5 encodes YCrCb, 4:2:2 digital video into the 720p, 1080i, 480p and 576p standards. All NTSC, PAL, or SECAM TV standards for interlaced output are also supported. CVE5 supports vertical blanking interval (VBI) encoding, including closed caption, teletext, WSS and CGMS-A encoding.

The CVE5 High Definition video encoder greatly reduces the risk and time involved when integrating this function into an IC. When combined with Zoran's Frame-It-1 Video Deinterlacer, CVE5 provides a quality solution for high definition video encoding.

Six separate output busses for Y, Composite, Chroma, and RGB provide for flexibility in connection and multiplexing to DACs.

Features

- 720p, 1080i, 480p and 576p standards supported
- Encodes 4:2:2 YCrCb into all variations of NTSC, PAL or SECAM interlaced TV standards for interlaced output
- Simultaneous output of composite video, S-video and component video supported
- Dual chroma paths for optimal output of both composite video and S-Video component video
- CCIR 601, 604 and 656 and SMPTE 253 standards supported
- 47-tap luma filter

- Outputs 10-bit data to DACs
- Vertical Blanking Interval (VBI) encoding support
- Closed caption, teletext, WSS & CGMS-A encoding
- Uniform 54 MHz clock; fully synchronous design
- 4x oversampling of luminance and chrominance filter for interlace mode
- 2x oversampling for progressive scan mode
- Process technology independent "softcore"

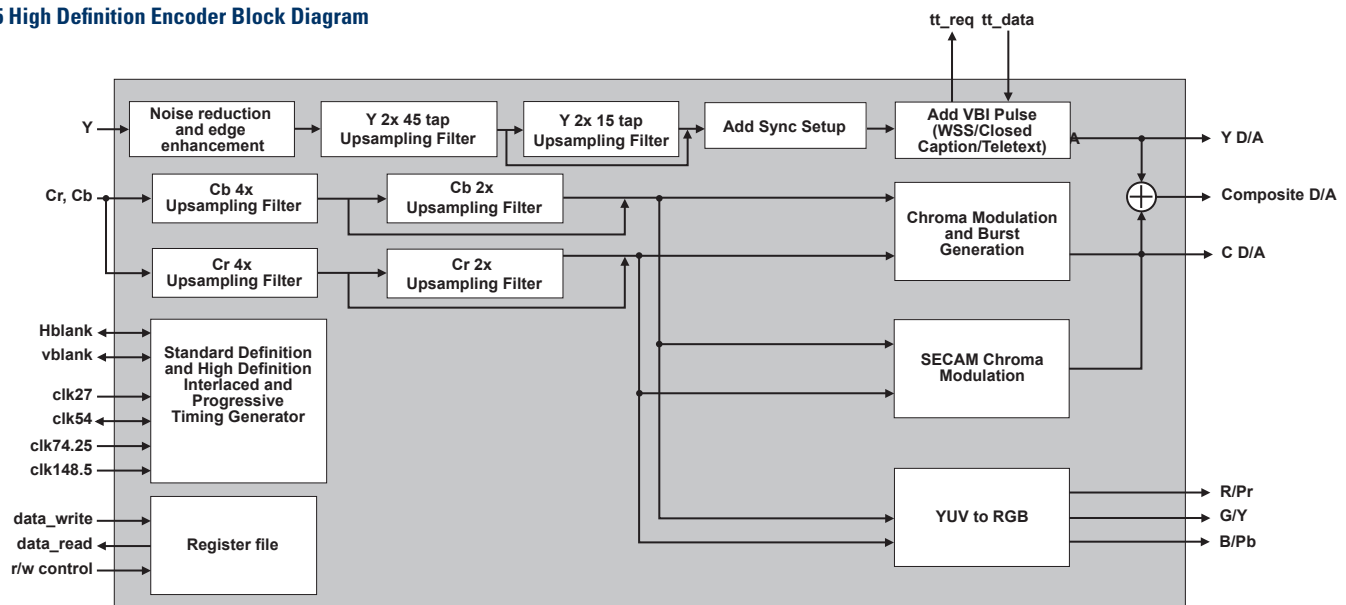
Integrated Circuit Applications

- HDTV
- Digital TV
- Set top box decoders
- Any system requiring high definition TV encoding

Deliverables

- Compilable Verilog source code
- Bit accurate, cycle accurate C model
- Synopsis synthesis scripts
- Test input files
- Documentation

CVE5 High Definition Encoder Block Diagram



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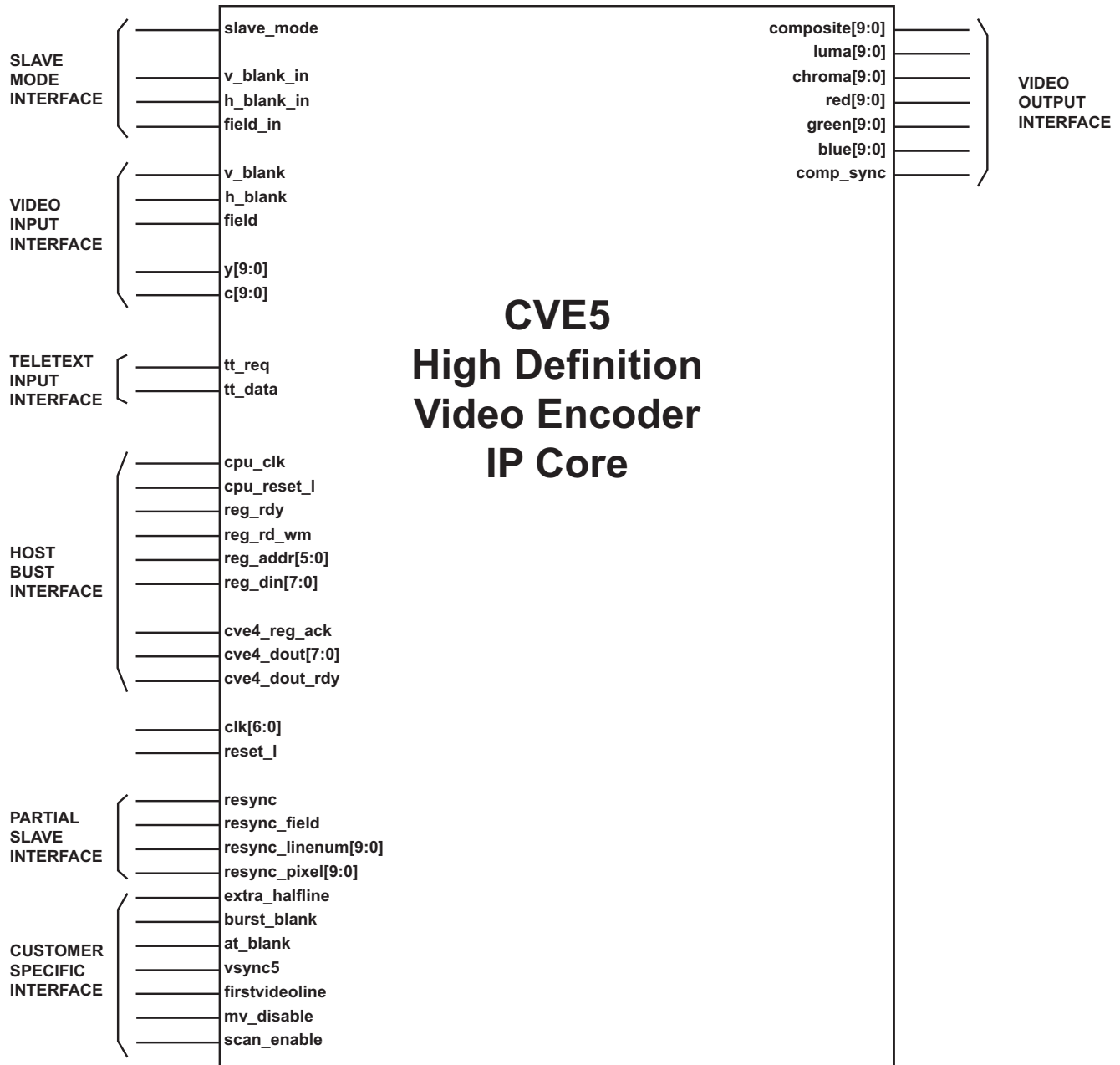
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CVE5 High Definition Encoder Logical Pinout



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